CLAIMS

1. An apparatus comprising:

a delay-locked loop circuit to generate a first clock signal, the delay-locked loop circuit including a first delay element coupled in a feedback path of the delay-locked loop circuit to advance the first clock signal relative to a reference clock signal by a first time period; and

a second delay element coupled to receive the first clock signal from the delay-locked loop circuit and to output a second clock signal that is delayed relative to the first clock signal by the first time period wherein the second delay element is outside the feedback path.

2. An apparatus as recited in claim 1 wherein the delay-locked loop circuit further includes a phase detector to identify phase differences between the first clock signal and the reference clock signal.

3. An apparatus as recited in claim 2 wherein the phase detector is a zero phase detector.

4. An apparatus as recited in claim 2 wherein the phase detector is an integration sampler to integrate the first clock signal with respect to the reference clock signal.

5. An apparatus as recited in claim 1 wherein the delay-locked loop circuit further includes a 180 degree phase shifter to adjust the phase of the first clock signal.

6. An apparatus as recited in claim 1 wherein the first clock signal indicates when to transmit data onto a data bus.

7. An apparatus as recited in claim 1 wherein the second clock signal indicates when to receive data from a data bus.

8. An apparatus as recited in claim 1 wherein the second delay element is separate from the delay-locked loop circuit.

9. A method comprising:

generating a first clock signal using a delay-locked loop circuit;

advancing the first clock signal relative to a reference clock signal by a first time period using a first delay element coupled in the feedback path of the delay-locked loop circuit; and

generating a second clock signal that is delayed relative to the first clock signal by the first time period using a second delay element coupled to receive the first clock signal, wherein the second delay element is outside the feedback path of the delay-locked loop circuit.

10. A method as recited in claim 9 further including transmitting data onto a data bus based on the state of the first clock signal.

11. A method as recited in claim 9 further including receiving data from a data bus based on the state of the first clock signal.

12. A method as recited in claim 9 further including identifying the phase differences between the first clock signal and the reference clock signal.

13. A method as recited in claim 9 further including integrating the first clock signal with respect to the reference clock signal.

14. A memory system comprising:

a memory storage device;

a data bus coupled to the memory storage device; and

a memory controller coupled to the data bus, the memory controller including:

a delay-locked loop circuit to generate a first clock signal, the delay-locked loop circuit including a first delay element coupled in a feedback path of the delay-locked loop circuit to advance the first clock signal relative to a reference clock signal by a first time period; and

a second delay element coupled to receive the first clock signal from the delay-locked loop circuit and to output a second clock signal that is delayed relative to the first clock signal by the first time period, wherein the second delay element is outside the feedback path.

15. A memory system as recited in claim 14 wherein the delay-locked loop circuit includes a phase detector to identify phase differences between the first clock signal and the reference clock.

16. A memory system as recited in claim 15 wherein the phase detector is a zero phase detector.

17. A memory system as recited in claim 15 wherein the phase detector is an integration sampler to integrate the first clock signal against the reference clock signal.

18. A memory system as recited in claim 14 wherein the first clock signal indicates when to transmit data onto the data bus.

19. A memory system as recited in claim 14 wherein the second clock signal indicates when to receive data from the data bus.

20. A memory system as recited in claim 14 wherein the second delay element is separate from the delay-locked loop circuit.